CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of improving the performance of different semiconductor conductivities on the same wafer comprising steps of

fabricating thin spacers on a wafer adjacent a gate structure,

depositing a hard mask film across said wafer,

forming a block mask over a first transistor,

removing said hard mask film from a second transistor,

forming a raised source-drain region by selective epitaxy,

removing said block mask over said first transistor,

performing additional selective epitaxial growth, effecting only the areas of said second transistor as said hard mask film covering said first transistor is resistant to said additional epitaxial procedure, and

performing extension implants to RSD regions of at least one of said first or second transistor.

2. A method as recited in claim 1 in which said performance improvements include at least one of

reducing series resistance,

subjecting extensions to low thermal budget processing only,

providing independent offset for said first and second transistors.

3. A method as recited in claim 1 wherein said first transistor is an nFET, and said second transistor is a pFET.

4. A method as recited in claim 3 wherein said wafer is an SOI wafer.

5. A method as recited in claim 1 wherein said thin spacers are comprised of an SiN film followed by a SiN spacer etch, wherein a thin SiO2 liner may be deposited prior to said SiN film and said SiN spacer etch with the resulting thickness of the spacer ranging from 3-15 nm.

6. A method as recited in claim 5 comprising the further steps of removing the hard mask from said first transistor, defining a block mask protecting said second transistor, implanting extensions to said first transistor, removing the block mask from said second transistor, defining a block mask protecting said first transistor, and implanting extensions to said second transistor.

7. A method as recited in claim 6 further comprising the step of fabricating source-drain spacers.

8. A method as recited in claim 7 further comprising the steps of

applying a first block mask over said second transistor,

performing source-drain implants to said first transistor,

removing said first block mask from said second transistor,

applying a second block mask over said first transistor,

performing source-drain implants to said second transistor, and

removing said second block mask from said first transistor.

9. A semiconductor apparatus comprising

a MOSFET device including Si wafer thinning, isolation, gate dielectric, and gate stack patterning,

a first transistor,

a second transistor,

thin sidewall spacers,

a thin epitaxial Si layer adjacent said thin sidewall spacers of a first transistor, and

a thick epitaxial Si layer in the extension region of a second transistor.

10. An apparatus as recited in claim 9 wherein said MOSFET device is an ultra-thin Si channel MOSFET.

11. An apparatus as recited in claim 9 further comprising a block film stack over the first transistor.

12. An apparatus as recited in claim 9 further comprising halo and extension implants in the region of the first transistor.

13. An apparatus as recited in claim 12 further comprising halo and extension implants in the region of the second transistor.

14. An apparatus as recited in claim 13 further comprising a source-drain spacers for said first and second transistors.

15. An apparatus as recited in claim 14 further comprising source-drain implants in regions of both first and second transistors.